AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. (Withdrawn) An orthogonal code generation apparatus generating an orthogonal code used in a spreading operation of data, comprising:

a signal source supplying a sequence number of n (n is a positive integer) bits specifying an orthogonal code sequence to be generated among a plurality of orthogonal code sequences defined based on a predetermined orthogonal code generation rule, and a location number of n bits specifying a position of an orthogonal code to be sequentially generated from said specified orthogonal code sequence;

a first logic operation circuit generating an element code by sequentially applying logic operation on the least significant bit of said sequence number and the least significant bit of said location number;

wherein said plurality of orthogonal code sequences are entirely defined by repeatedly arranging a combination of element codes that can be generated by logic operation on said least significant bits and an inverted version of said combination, based on a pattern of said combination of element codes,

a second logic operation circuit sequentially applying logic operation on (n – 1) bits of said sequence number excluding the least significant bits and (n – 1) bits of said location number excluding the least significant bit; and

a select circuit selecting, based on an arrangement of said combination, either said element code generated by said first logic operation circuit or an inverted code of said generated element code in response to a computation result of said second logic operation circuit, and providing the selected code as said orthogonal code.

2. (Withdrawn) The orthogonal code generation apparatus according to claim 1, wherein said first logic operation circuit includes an AND circuit sequentially ANDing the least significant bit of said sequence number and the least significant bit of said location number to sequentially generate the ANDed value as said element code,

wherein said combination of element codes that can be generated includes three codes "0" and one code "1", and said inverted version of combination includes three codes "1" and one code "0".

3. (Withdrawn) The orthogonal code generation apparatus according to claim 2, wherein said second logic operation circuit includes a determination circuit determining whether the number of digits where both of corresponding digits take a value of 1 between (n – 1) bits of said sequence number excluding the least significant bit and (n – 1) bits of said location number excluding the least significant bit is 0 or an even number, or an odd number,

wherein said select circuit selects as an orthogonal code an element code generated by said AND circuit when a determination result of said determination circuit exhibits 0 or an even

number, and selects as an orthogonal code an inverted code of said element code when said determination result exhibits an odd number.

4. (Withdrawn) The orthogonal code generation apparatus according to claim 3, wherein said determination circuit comprises

(n – 1) AND circuits ANDing values in corresponding digits between (n – 1) bits of said sequence number excluding the least significant bit and (n – 1) bits of said location number excluding the least significant bit, and

an adder circuit adding the AND results of said (n – 1) AND circuits, and generating a control signal indicating whether the result of addition is 0 or an even number, or an odd number.

5. (Withdrawn) The orthogonal code generation apparatus according to claim 1, further comprising a location number modify circuit modifying arrangement of predetermined bits among said supplied location number of n bits.

6. (Withdrawn) The orthogonal code generation apparatus according to claim 5, wherein repetition of an arrangement based on a pattern of said combination of element codes is defined with a period index k (k is a positive integer), the number of said plurality of orthogonal code sequences being represented by 2^k, and the number of bits of each of said plurality of orthogonal code sequences being represented by 2^k,

wherein said location number modify circuit modifies arrangement of the lower k bits of said location number of n bits so as to be in reverse order from the least significant bit to the k-th bit.

7. (Withdrawn) A portable radio terminal of digital radio communication, comprising:

a modem processing data for transmission and reception; and

a radio processor applying processing for radio communication on transmission data of said modem and sending out the processed data as a transmission radio signal, and applying processing for radio communication on a received reception radio signal to apply the processed signal to said modem as reception data;

wherein said modem includes an orthogonal code generation apparatus generating an orthogonal code used in a spreading operation of said data,

said orthogonal code generation circuit comprising:

a signal source supplying a sequence number of n (n is a positive integer) bits specifying an orthogonal code sequence to be generated among a plurality of orthogonal code sequences defined based on a predetermined orthogonal code generation rule, and a location number of n bits specifying a position of an orthogonal code to be sequentially generated from said specified orthogonal code sequence;

a first logic operation circuit generating an element code by sequentially applying logic operation on the least significant bit of said sequence number and the least significant bit of said location number;

wherein said plurality of orthogonal code sequences are entirely defined by repeatedly arranging a combination of element codes that can be generated by logic operation on said least significant bits and an inverted version of said combination, based on a pattern of said combination of element codes,

a second logic operation circuit sequentially applying logic operation on (n – 1) bits of said sequence number excluding the least significant bits and (n – 1) bits of said location number excluding the least significant bit; and

a select circuit selecting, based on an arrangement of said combination, either said element code generated by said first logic operation circuit or an inverted code of said generated element code in response to a computation result of said second logic operation circuit, and providing the selected code as said orthogonal code.

8. (Withdrawn) The portable radio terminal according to claim 7, wherein said first logic operation circuit includes an AND circuit sequentially ANDing the least significant bit of said sequence number and the least significant bit of said location number to sequentially generate the ANDed value as said element code,

wherein said combination of element codes that can be generated includes three codes "0" and one code "1", and said inverted version of combination includes three codes "1" and one code "0".

9. (Withdrawn) The portable radio terminal according to claim 8, wherein said second logic operation circuit includes a determination circuit determining whether the number of digits where both of corresponding digits take a value of 1 between (n – 1) bits of said sequence number excluding the least significant bit and (n – 1) bits of said location number excluding the least significant bit is 0 or an even number, or an odd number,

wherein said select circuit selects as an orthogonal code an element code generated by said AND circuit when a determination result of said determination circuit exhibits 0 or an even number, and selects as an orthogonal code an inverted code of said element code when said determination result exhibits an odd number.

10. (Withdrawn) The portable radio terminal according to claim 9, wherein said determination circuit comprises

(n – 1) AND circuits ANDing values in corresponding digits between (n – 1) bits of said sequence number excluding the least significant bit and (n – 1) bits of said location number excluding the least significant bit, and

an adder circuit adding the AND results of said (n – 1) AND circuits, and generating a control signal indicating whether the result of addition is 0 or an even number, or an odd number.

11. (Withdrawn) The portable radio terminal according to claim 7, further comprising a location number modify circuit modifying arrangement of predetermined bits among said supplied location number of n bits.

12. (Withdrawn) The portable radio terminal according to claim 11, wherein repetition of an arrangement based on a pattern of said combination of element codes is defined with a period index k (k is a positive integer), the number of said plurality of orthogonal code sequences being represented by 2^k, and the number of bits of each of said plurality of orthogonal code sequences being represented by 2^k,

wherein said location number modify circuit modifies arrangement of the lower k bits of said location number of n bits so as to be in reverse order from the least significant bit to the k-th bit.

13. (Previously Presented) A scrambling code generation apparatus generating a scrambling code used in a scrambling operation of transmission data, comprising:

a shift register formed of a plurality of stages of registers connected so as to execute a feedback operation and a spreading operation to generate a sequence of scrambling codes by a predetermined generating polynomial;

an arithmetic circuit computing values of said registers involved with said feedback operation and said spreading operation that would have been obtained if said shift register carries out a shift operation for an increasing predetermined number of times based on predetermined initial values;

an input circuit applying said computed values of registers into corresponding said registers; and

a control circuit controlling said arithmetic circuit and said input circuit so that said arithmetic circuit computes values of said registers and said input circuit applies said computed values into said registers until all said plurality of stages of registers store valid values based on said computed values and said input values;

wherein said shift register continues a shift operation based on valid values stored in all of said plurality of stages of registers to generate said sequence of scrambling codes.

14. (Original) The scrambling code generation apparatus according to claim 13, further comprising:

a storage circuit storing said predetermined initial values; and

a matrix supply circuit supplying a matrix to determine values of registers involved with said feedback operation and said spreading operation after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial,

wherein said arithmetic circuit multiplies said predetermined initial values stored in said storage circuit by said matrix supplied from said matrix supply circuit to compute values of said registers.

15. (Original) The scrambling code generation apparatus according to claim 13, further comprising a storage circuit storing said predetermined initial values,

wherein said arithmetic circuit obtains by a predetermined operation a matrix to determine values of registers involved with said feedback operation and said spreading operation

after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial, and multiplying by said predetermined initial values stored in said storage means to compute values of said registers.

16. (Currently Amended) A scrambling code generation apparatus generating a scrambling code used in a scrambling operation of transmission data, comprising:

a storage circuit storing predetermined initial values;

a logic circuit producing a matrix by a predetermined operation, said matrix being used to determine a value of each code forming a sequence of scrambling codes based on a predetermined generating polynomial; and

an arithmetic circuit ~~multiplying~~ that receives said matrix produced by the logic circuit as an input, multiplies said predetermined initial values stored in said storage circuit by said matrix produced by said logic circuit to compute a value of each code forming said sequence of scrambling codes, and outputs said sequence of scrambling codes.

17. (Previously Presented) A portable radio terminal of digital radio communication, comprising:

a transmission related modem modulating transmission data; and

a radio processor applying processing for radio communication on transmission data of said transmission related modem to send out the processed data as a transmission radio signal;

said transmission related modem comprising a scrambling code generation apparatus generating a scrambling code used in a scrambling operation of said transmission data,

said scrambling code generation apparatus comprising:

a shift register formed of a plurality of stages of registers connected so as to execute a feedback operation and a spreading operation to generate a sequence of scrambling codes by a predetermined generating polynomial;

an arithmetic circuit computing values of said registers involved with said feedback operation and said spreading operation that would have been obtained if said shift register carries out a shift operation for an increasing predetermined number of times based on predetermined initial values;

an input circuit applying said computed values of registers into corresponding said registers; and

a control circuit controlling said arithmetic circuit and said input circuit so that said arithmetic circuit computes values of said registers and said input circuit applies said computed values into said registers until all said plurality of stages of registers store valid values based on said computed values and said input values;

wherein said shift register continues a shift operation based on valid values stored in all of said plurality of stages of registers to generate said sequence of scrambling codes.

18. (Original) The portable radio terminal according to claim 17, further comprising:

a storage circuit storing said predetermined initial values; and

a matrix supply circuit supplying a matrix to determine values of registers involved with said feedback operation and said spreading operation after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial,

wherein said arithmetic circuit multiplies said predetermined initial values stored in said storage circuit by said matrix supplied from said matrix supply circuit to compute values of said registers.

19. (Original) The portable radio terminal according to claim 17, further comprising a storage circuit storing said predetermined initial values,

wherein said arithmetic circuit obtains by a predetermined operation a matrix to determine values of registers involved with said feedback operation and said spreading operation after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial, and multiplying by said predetermined initial values stored in said storage means to compute values of said registers.

20. (Currently Amended) A portable radio terminal of digital radio communication, comprising:

a transmission related modem modulating transmission data; and

a radio processor applying processing for radio communication on transmission data of said transmission related modem to send out the processed data as a transmission radio signal,

said transmission related modem comprising a scrambling code generation apparatus generating a scrambling code used in a scrambling operation of said transmission data,

said scrambling code generation apparatus comprising:

a storage circuit storing predetermined initial values,

a logic circuit producing a matrix by a predetermined operation, said matrix being used to determine a value of each code forming a sequence of scrambling codes based on a predetermined generating polynomial; and

an arithmetic circuit ~~multiplying~~ that receives said matrix produced by the logic circuit as an input, multiplies said predetermined initial values stored in said storage circuit by said matrix produced by said logic circuit to compute a value of each code forming said sequence of scrambling codes, and outputs said sequence of scrambling codes.